

This cross-sectional view illustrates a semiconductor device. A substrate 110 of P-TYPE is shown at the bottom. A trench isolation structure 112 is formed in the substrate, with its sidewalls labeled 114. The bottom of the trench is labeled 116. A gate stack 122 is positioned on top of the substrate, spanning across the trench. The gate stack consists of a gate oxide layer 120A and 120B, and a gate electrode layer 132A and 132B. The width of the gate electrode is labeled W. A channel region 124 is formed in the substrate directly beneath the gate electrode. The channel region is doped with n+ ions, as indicated by the label n+. The channel region is bounded by sidewall spacers 126A and 126B. The entire device is covered by a top layer 136.

FIG. 1B

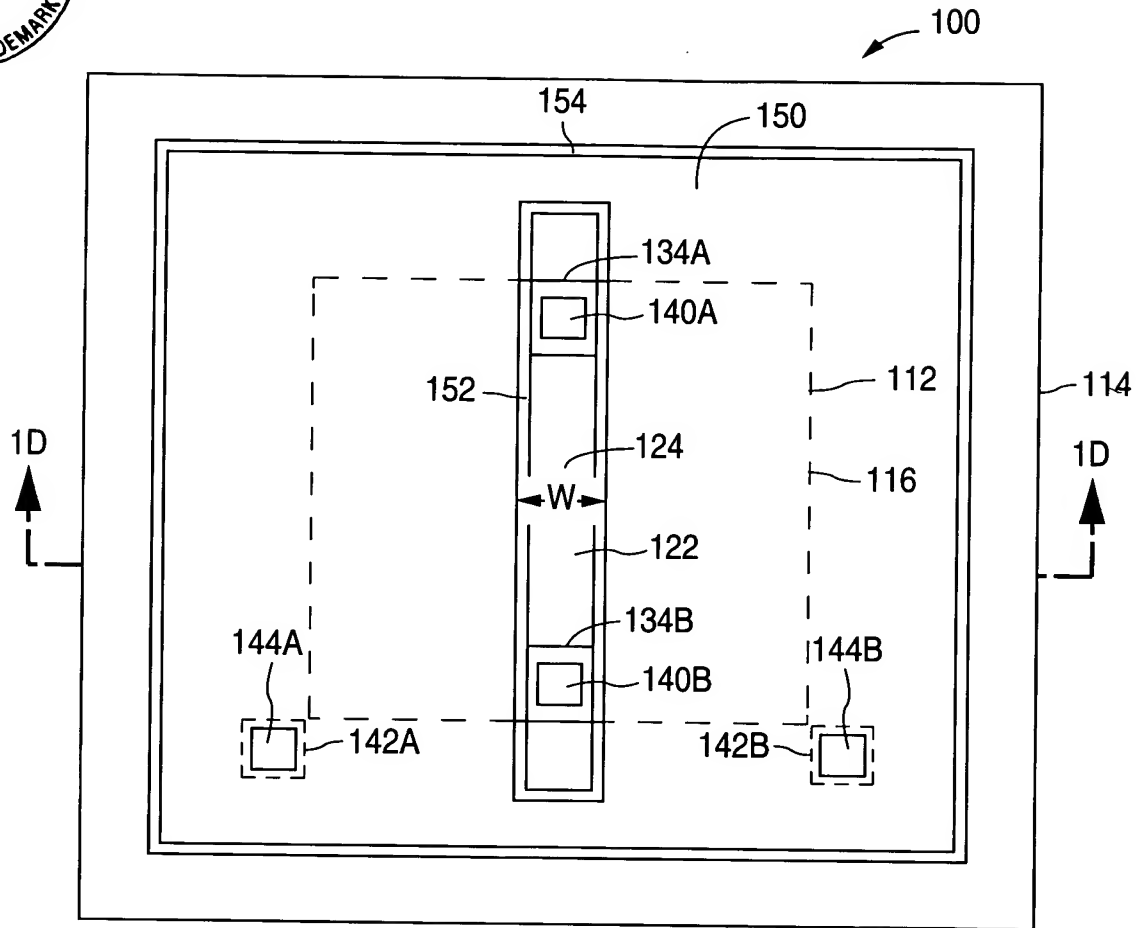


FIG. 1C

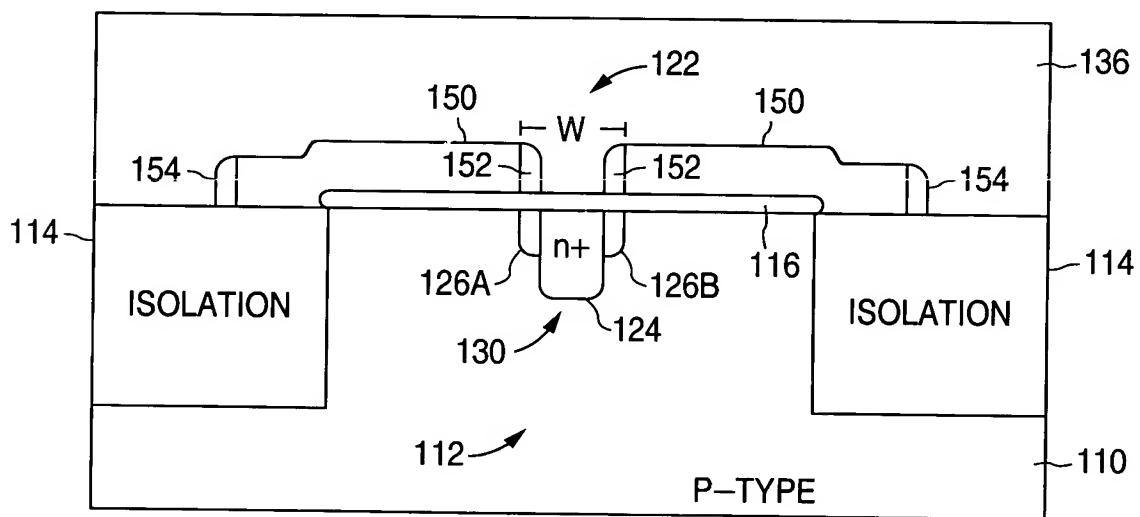
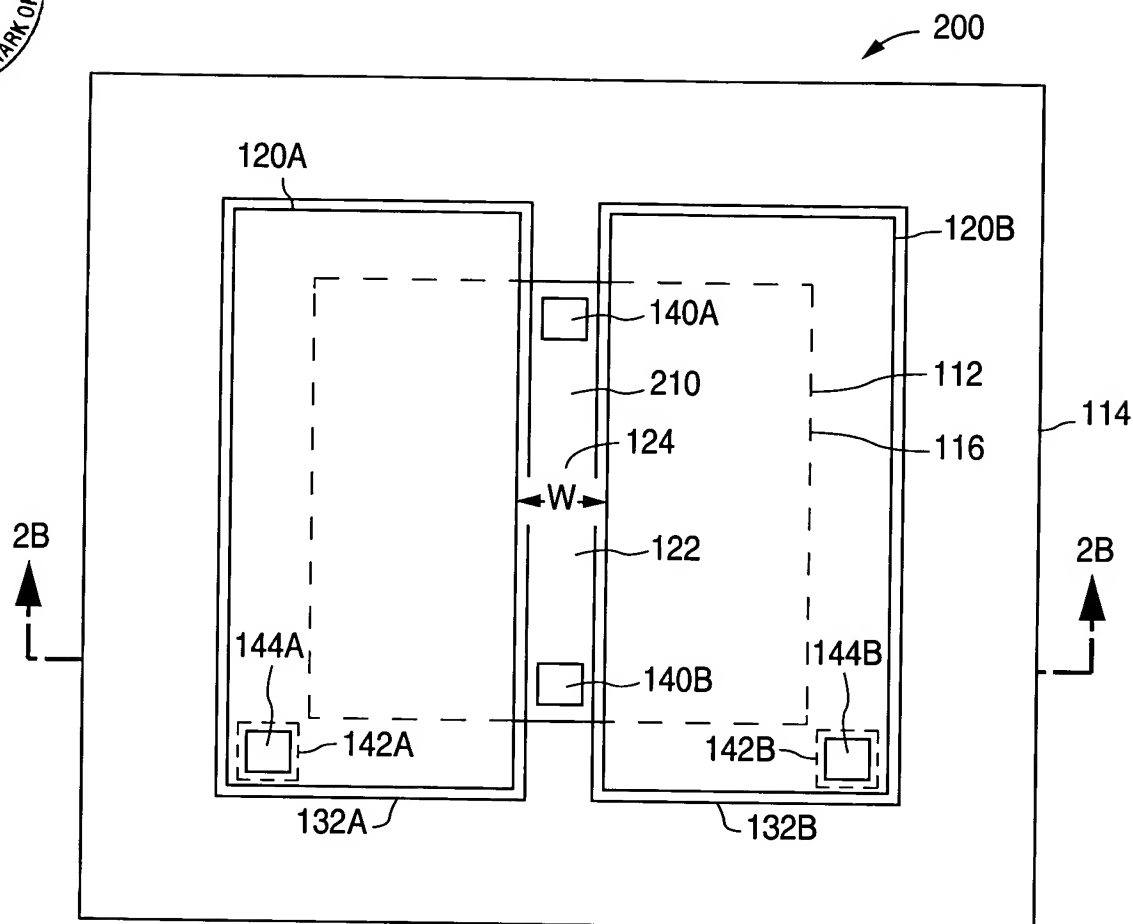
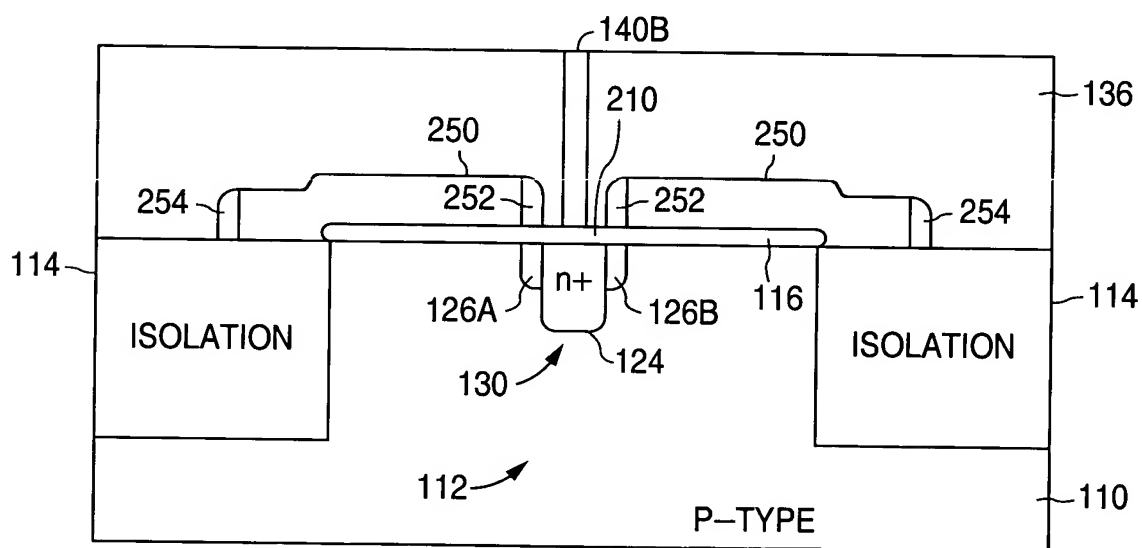
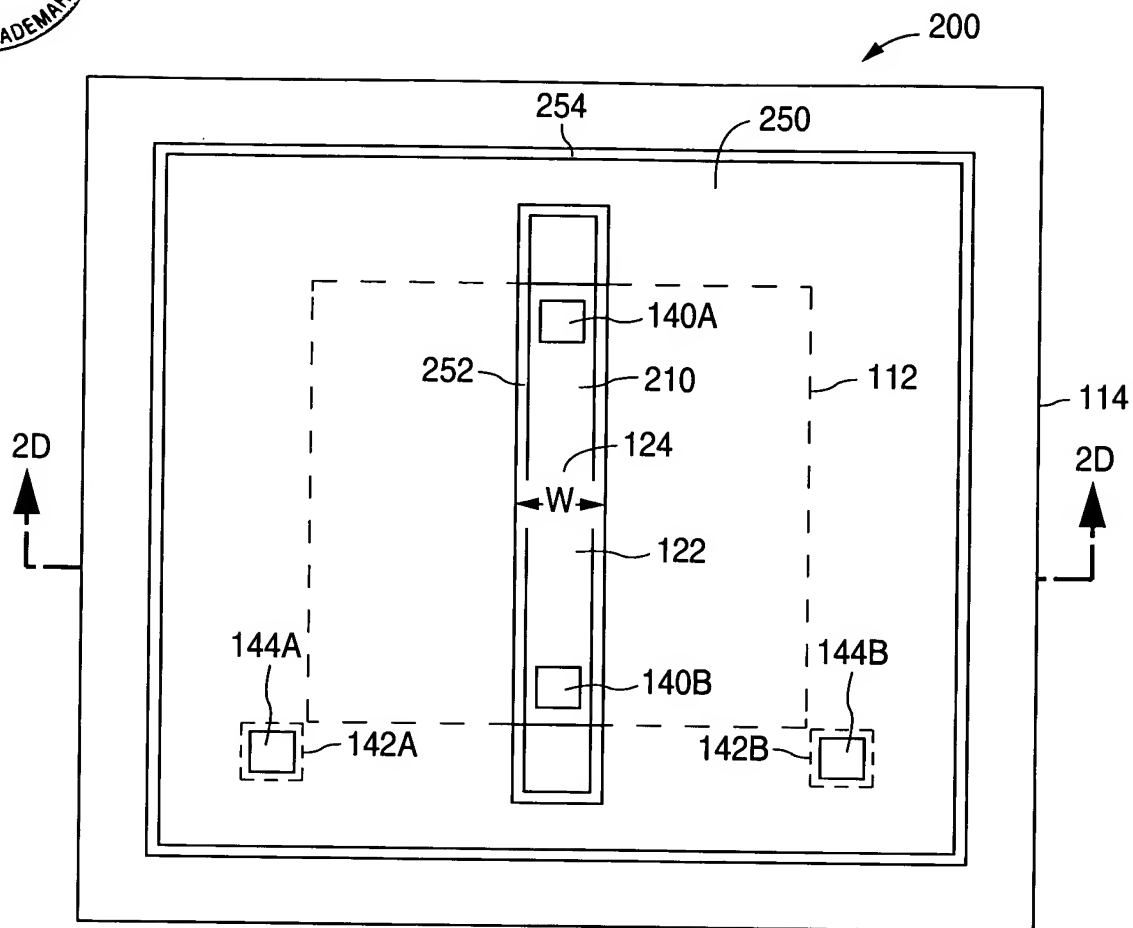


FIG. 1D



This cross-sectional view illustrates a semiconductor device with a trench isolation structure. The device is built on a P-TYPE substrate (110). A trench (112) is formed in the substrate, and its sidewalls are covered by an isolation layer (114). The trench is filled with a conductive material (116). A gate stack (120A, 120B) is formed on the top surface of the substrate, with a gate oxide layer (126A, 126B) and a gate electrode (124). A source/drain region (130) is formed in the substrate, with a source/drain oxide layer (132A, 132B) and a source/drain electrode (136). A trench (140B) is formed in the gate stack, and its sidewalls are covered by a trench oxide layer (140A).

FIG. 2B



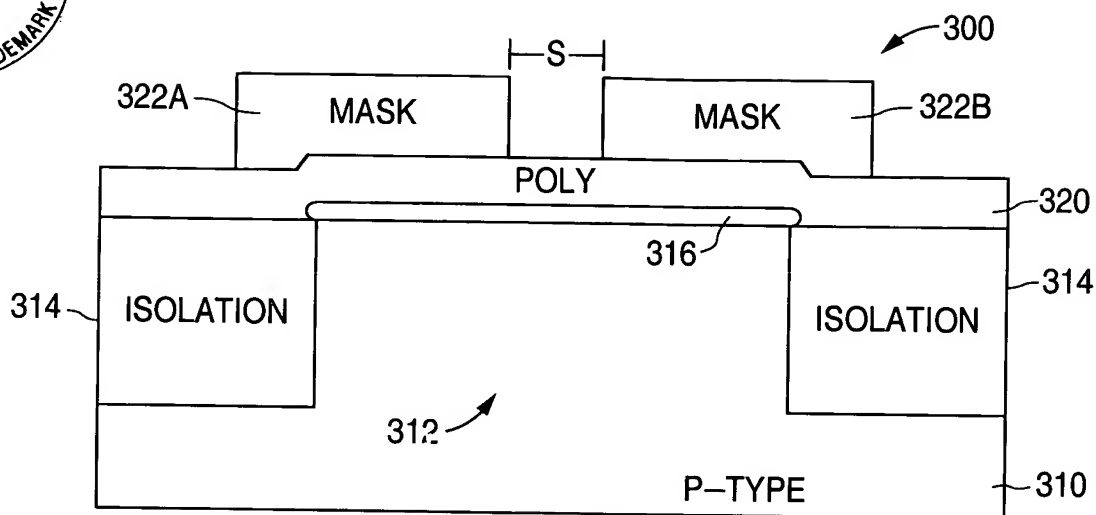


FIG. 3A

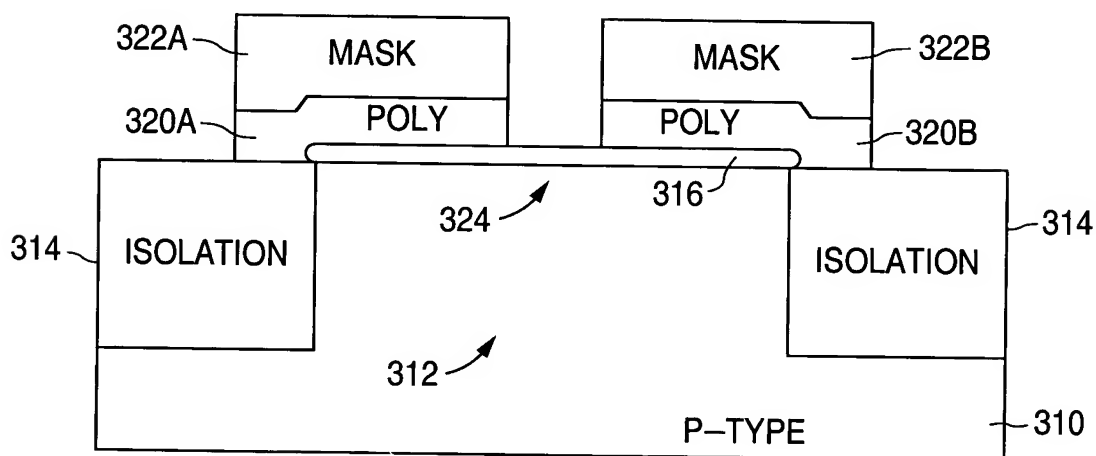


FIG. 3B

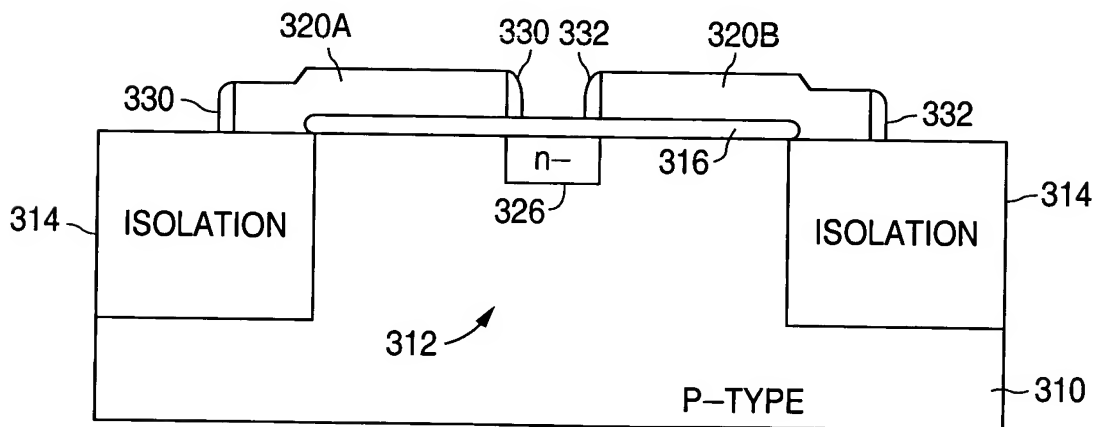


FIG. 3C

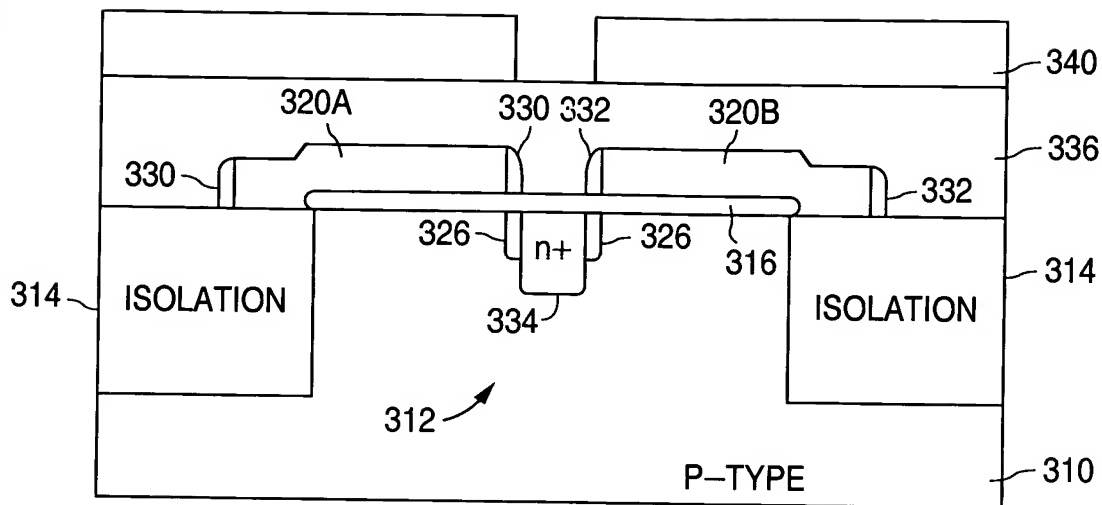


FIG. 3D

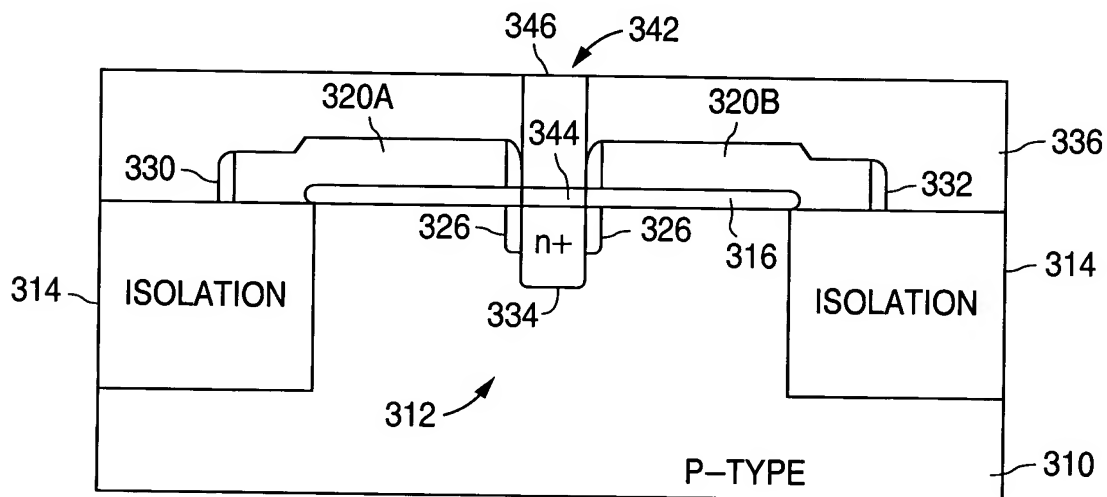


FIG. 3E

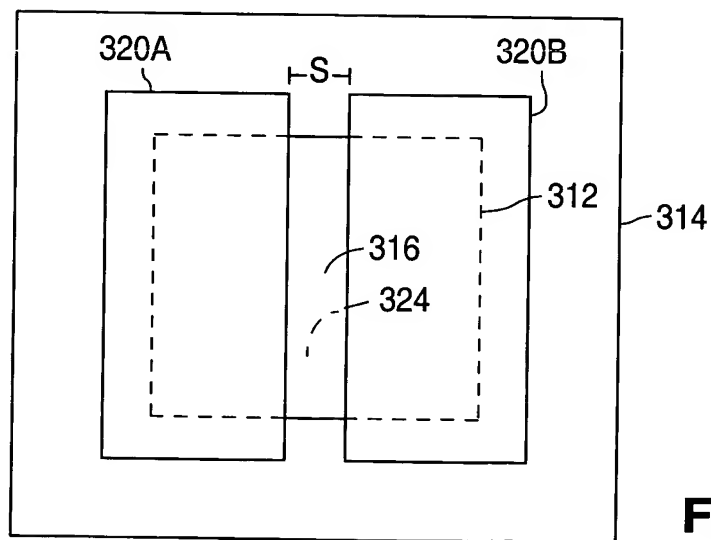


FIG. 4

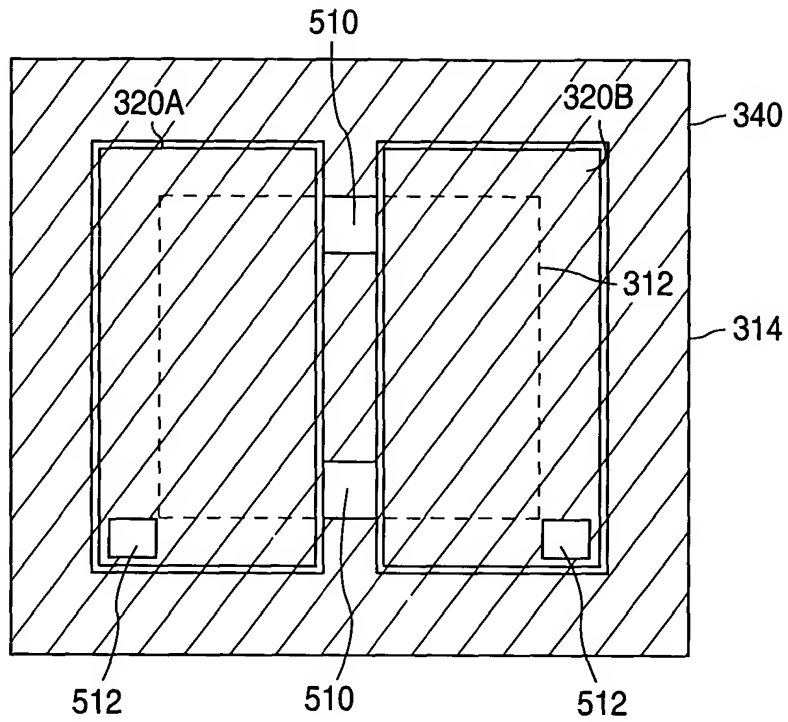


FIG. 5

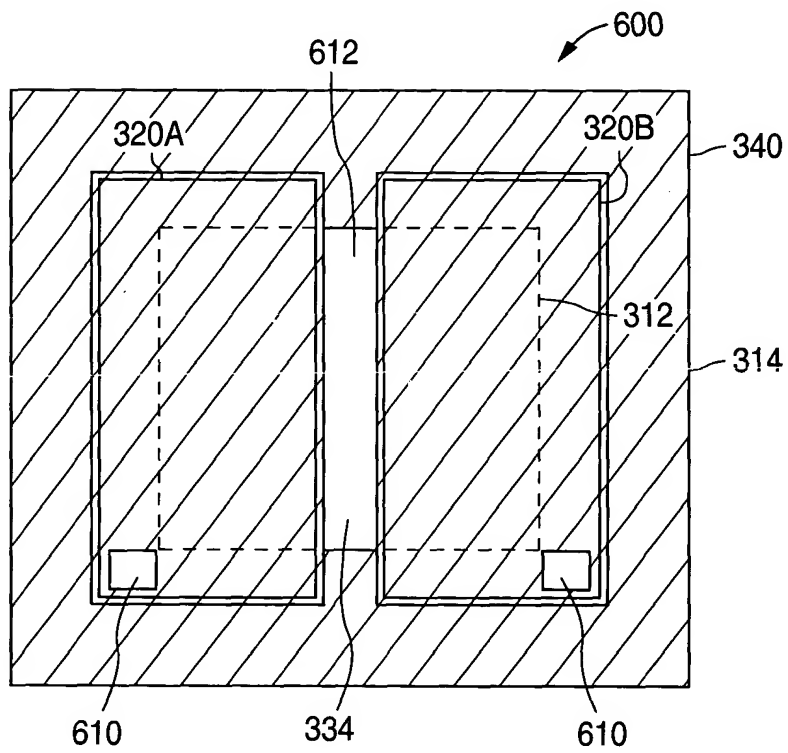


FIG. 6